QUARTERLY TECHNICAL REPORT

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FOREWORD

This report covers work performed for the Jet Propulsion Laboratory, California Institute of Technology (under JPL Contract 951079) which is sponsored by the National Aeronautics and Space Administration under NASA Contract NAS7-100.

CONTENTS

ILLUSTRATIONS

Section 1
PROGRAM OBJECTIVE AND SPECIFICATIONS

1.1 OBJECTIVE

The objective of this program is to design, fabricate, and test a subsystem consisting of an eight-pole commutator, an associated shift register, and control logic that will meet the functional, electrical, and environmental requirements defined in JPL Specification GMN-50524-DSN-A. The latest state-of-the-art developments in MOS technology are to be applied wherever possible.

1.2 FUNCTIONAL REQUIREMENTS

The following statement is quoted from JPL Specification GMN-50524-DSN-A which was enclosed in the Appendix of Quarterly Technical Report No. 1.

> "Functional requirements: The commutator shall function so that it switches sequentially each of eight analog voltage inputs to a common output line as illustrated in Fig. 1. A quaded deck switch shall be provided for the control of the analog voltage output. The commutator shall contain a second set of eight switches for multiplexing variable-resistance sensors (see Fig. 2). Certain logic functions shall be provided to control the operation of the shift register and the deck switch. Figure 1 illustrates the complete functional representation of the required logic with the following exception. If the shift register is designed with a logical delay between clock line activation (logic "1") and the activation of any stage output, an equivalent delay shall be provided in line X. This is necessary in order for the deck switch to be activated and deactivated in phase with the analog switches."

Section 2
PROGRAM DEFINITION

The steps listed below define the program which will be followed in order to develop and manufacture the required hardware:

1. Preliminary study
2. Design
   - Block diagram
   - Schematic diagram
   - Logic diagram
   - Timing diagram
3. Breadboard verification of design
4. Development of environmental test plan
5. Drafting — logic diagram and schematic diagram
6. Production of MOS composite
7. Production of masks
8. Evaluation run — pilot line
9. Testing of evaluation wafers
10. Final run — pre-production line
11. Testing of production wafers.

Section 3
STATUS REPORT

3.1 PRELIMINARY STUDY

During the preliminary study, the following areas required investigation and recommendations:

- type of shift register
- deck switch redundancy
- modification of manufacturing process
- analog switch saturation voltage
- time relationship of JPL logic inputs
- signal conditioning of JPL logic inputs.

3.1.1 Type of Shift Register

Three alternative shift register implementations were discussed in Section 3.1 of the first Quarterly Technical Report. Final choice has been made on the basis of device count and simplicity of interconnection. In order to utilize minimum chip area, thereby achieving maximum device manufacturing yields, the dynamic shift register was selected as the most suitable circuit. The three-phase clock required is shown in Fig. 3-1.

Circuit Operation. It may be seen in Fig. 3-2 that the change of ϕ_2 and ϕ_3 from negative to positive opens devices No. 4 and No. 7. Only after they have opened does ϕ_1 go negative, causing device 1 to close and enabling inputs to stage 1, stage 2, etc. When ϕ_1 goes positive, device No. 1 opens. Device No. 3 then holds its state due to the charge on its gate until ϕ_2 causes device No. 4 to close, passing the signal to device No. 6. The closing of device No. 7 then completes the loop and the stage is latched.

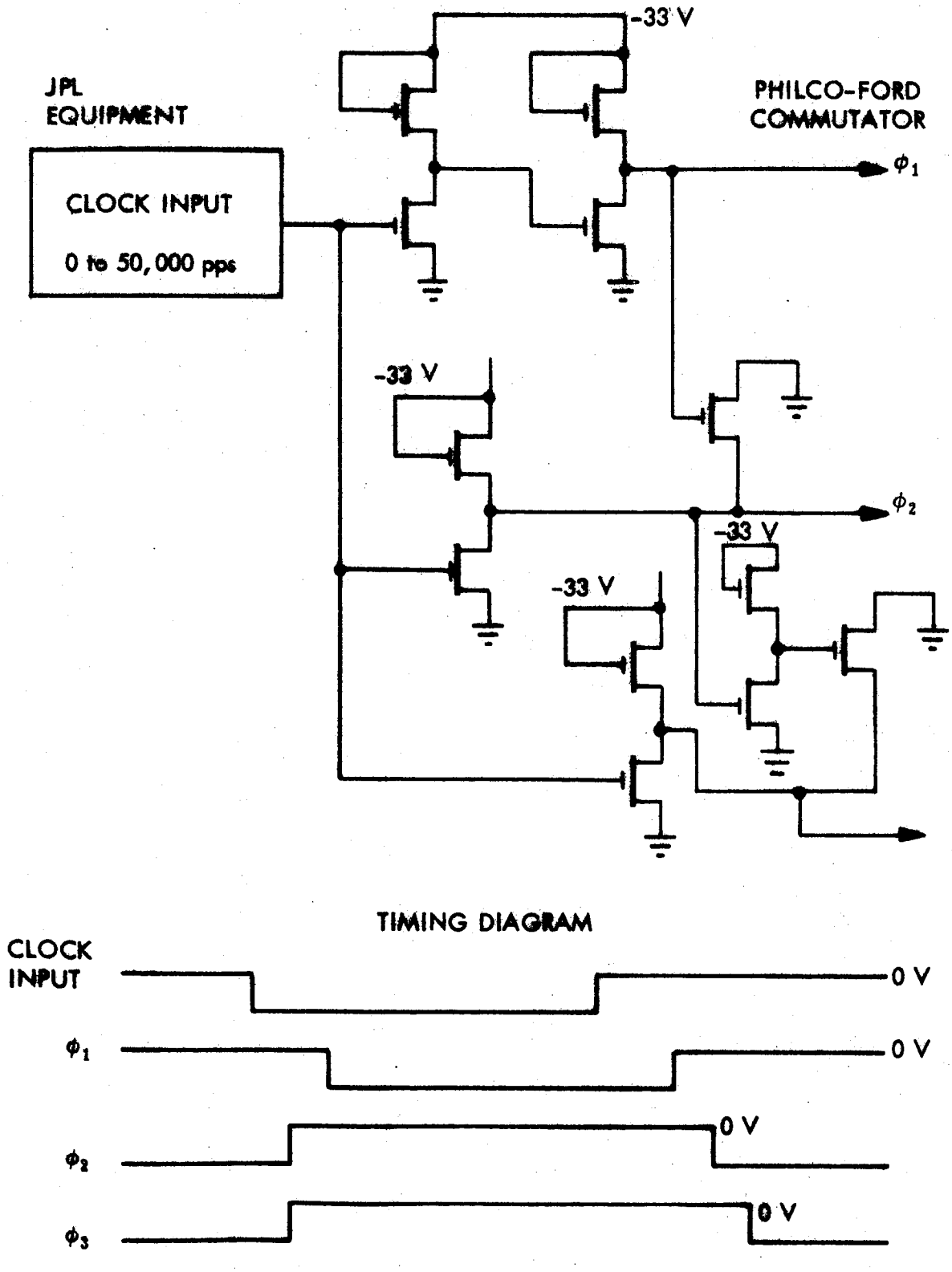


Fig. 3-1 Schematic Diagram of Three-Phase Clock

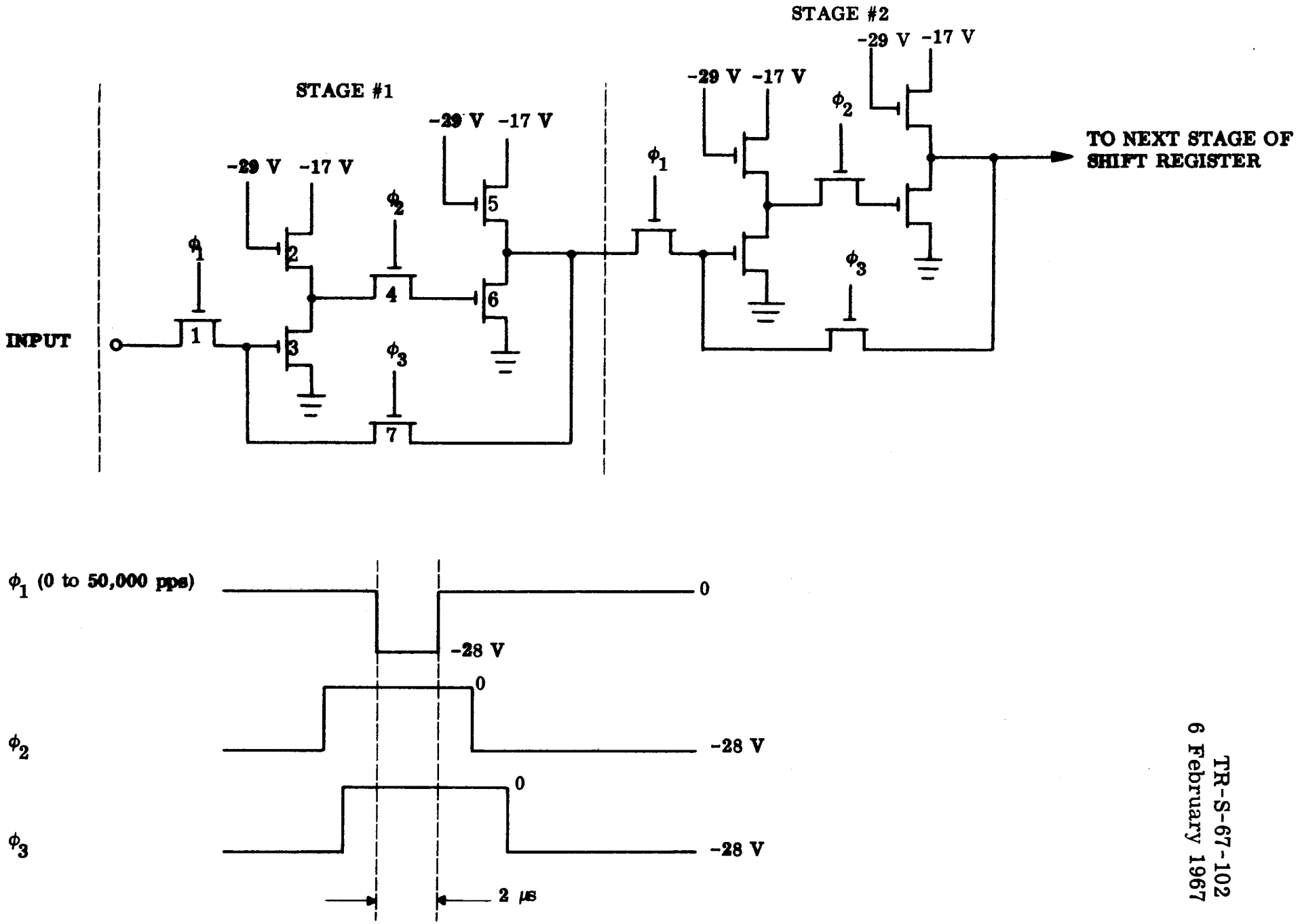


Fig. 3-2 Schematic Diagram and Timing of Dynamic Shift Register

3.1.2 Deck Switch Redundancy

Redundancy of the deck switch increases the area of the chip without actually preventing a drain-to-gate short on either of the two output devices closest to "Output C" as shown in Fig. 3-3. It is recommended that a single device be used and that appropriate burn-in be utilized to achieve the desired reliability.

3.1.3 Modification of Manufacturing Process

In Section 4 of the first Quarterly Technical Report the modified manufacturing process necessary to produce devices capable of withstanding 50-V levels was discussed. This process is now standard for all Philco-Ford MOS devices. Extensive testing has shown device characteristic improvement in several areas such as breakdown voltage and leakage current. Drain-to-source breakdown voltage of the JPL array will be specified in the 50- to 60-V range. Maximum allowable gate-to-P-region and gate-to-substrate voltages will be specified in the 40- to 50-V range.

3.1.4 Analog Switch Saturation Voltage

The data shown in graphs A2 through A10 of the Appendix indicate that a gate voltage of approximately -24 V will hold the analog switches in saturation when operated under the ambient temperature and power-supply voltage conditions specified by JPL.

The test sample used to derive the curves presented in the Appendix was eight thick-oxide Philco-Ford 1004 discrete MOS transistors. The ON resistance of all eight devices was within the limits shown on each graph.

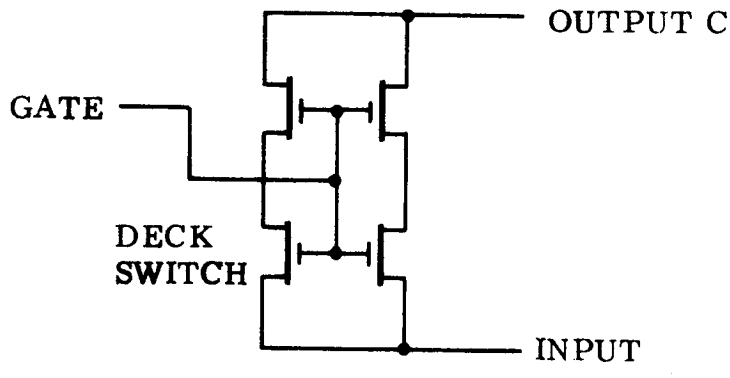


Fig. 3-3 Deck Switch

3.1.5 Time Relationship of JPL Logic Inputs

In order to specify the input logic relationships, JPL has agreed that at the output of the first NOR gate the clock will always lag the shift register input by 0.2 to 1.0 μs.

3.1.6 Signal Conditioning of JPL Logic Inputs

It may be seen in Fig. 3-4 that the register input changes state during the clock pulse of the 2^{nth} deck. If the JPL register input were to be fed directly to the input of the shift register, it is obvious that a malfunction would occur in the 2^{nth} deck. To prevent this fault condition, the circuit of Fig. 3-5 has been added. The circuit is designed so that the JPL register input is shifted only for the 2^{nth} deck (see Fig. 3-6). The signal conditioning circuit of Fig. 3-5 is an RS flip-flop with minor logic modifications. The schematic diagram of the JPL eight-pole commutator is shown in Fig. 3-7.

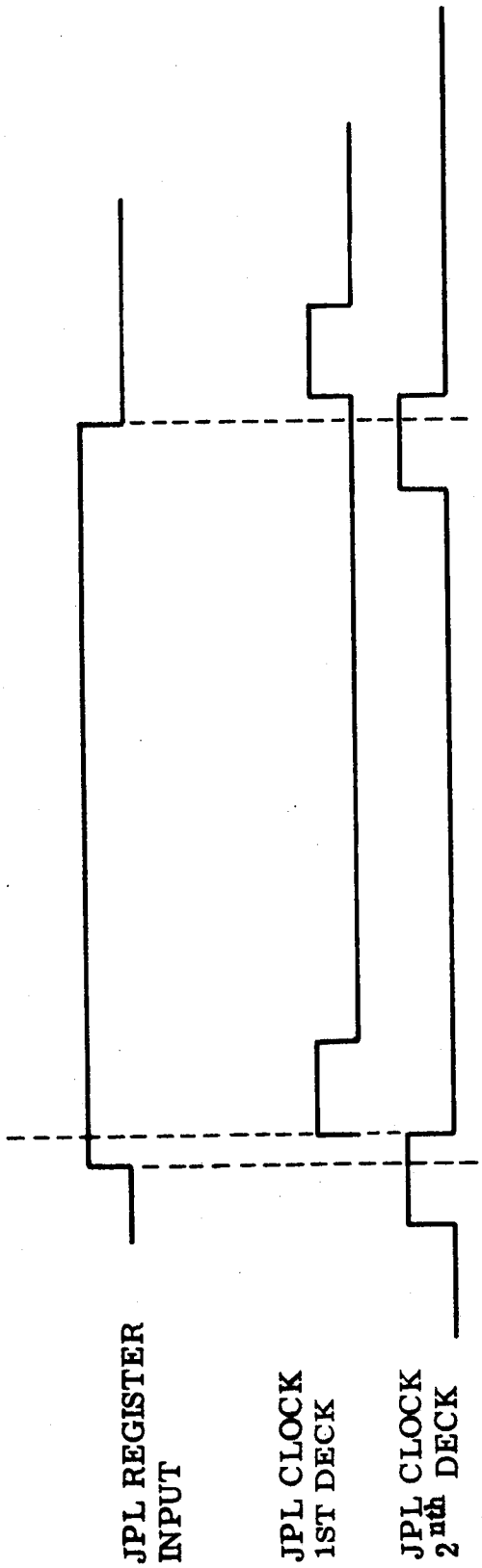


Fig. 3-4 Timing Diagram of JPL Inputs

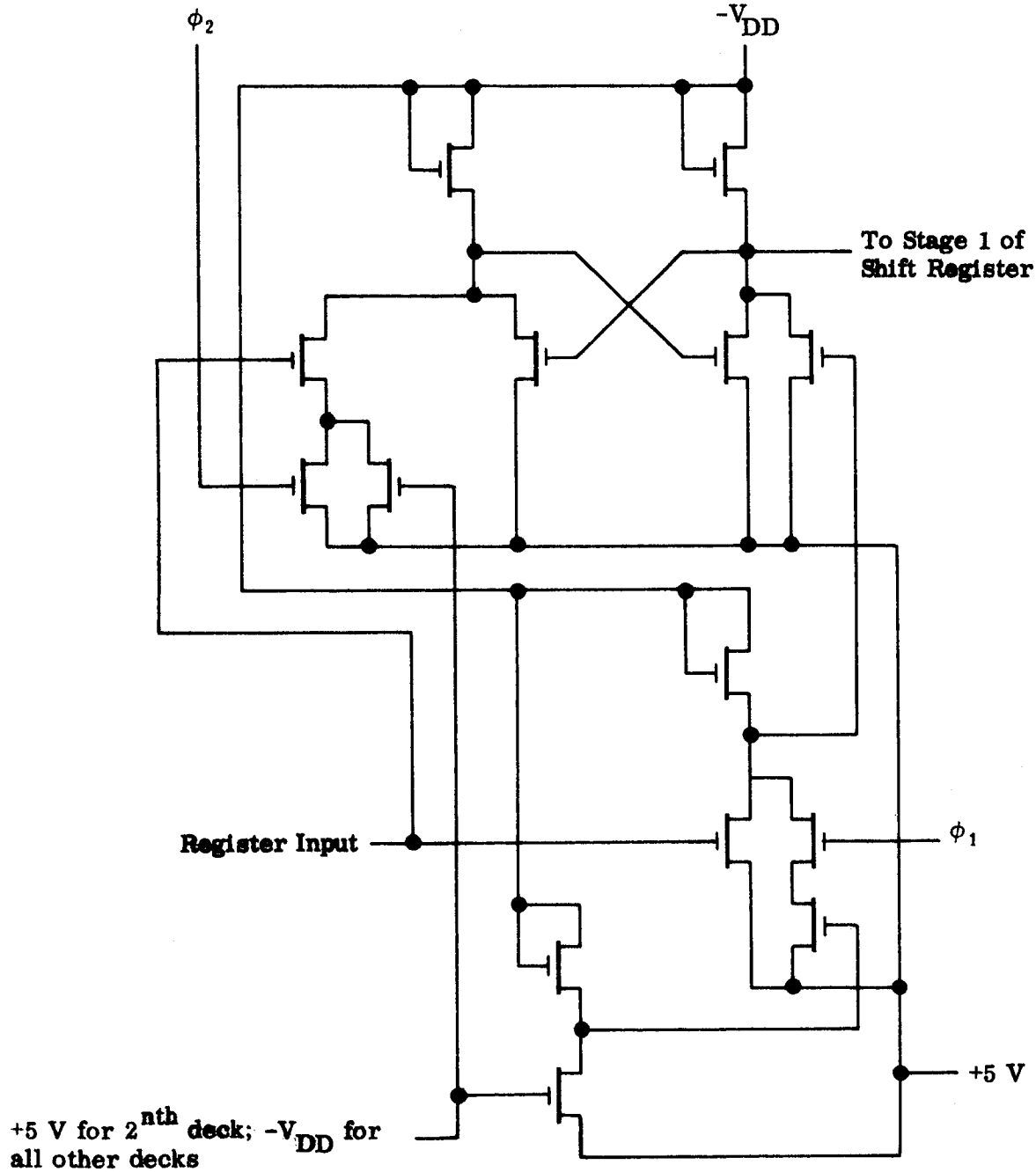


Fig. 3-5 Resistor Input Signal Conditioner

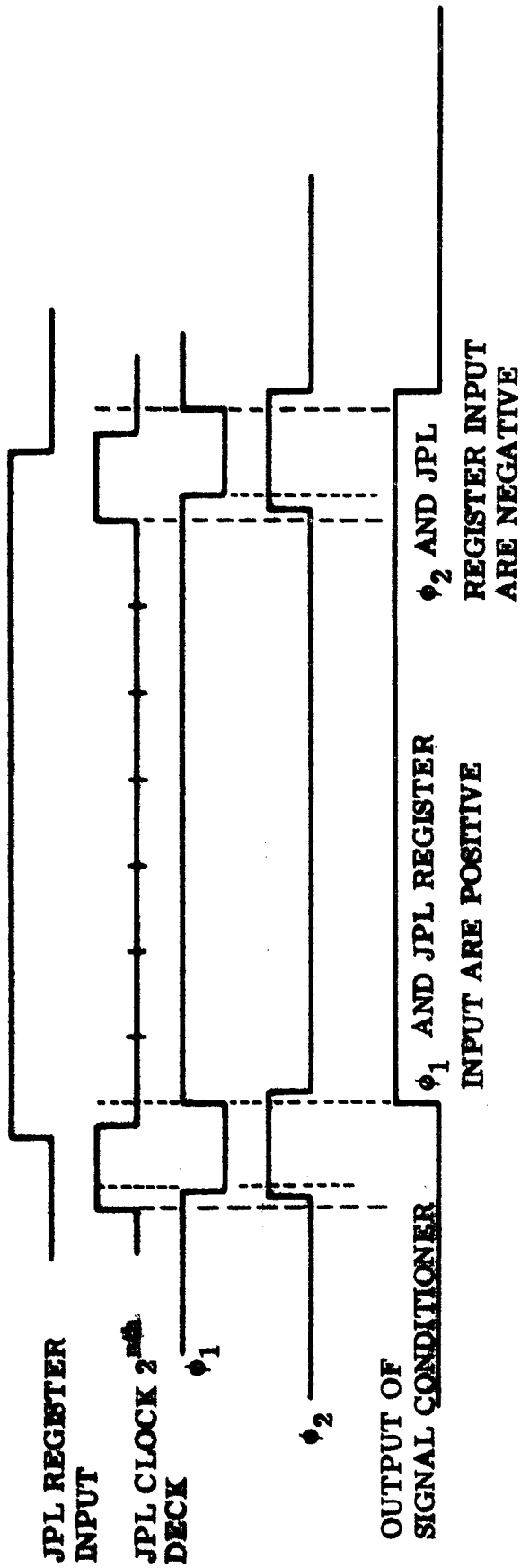


Fig. 3-6 Signal Conditioning Timing

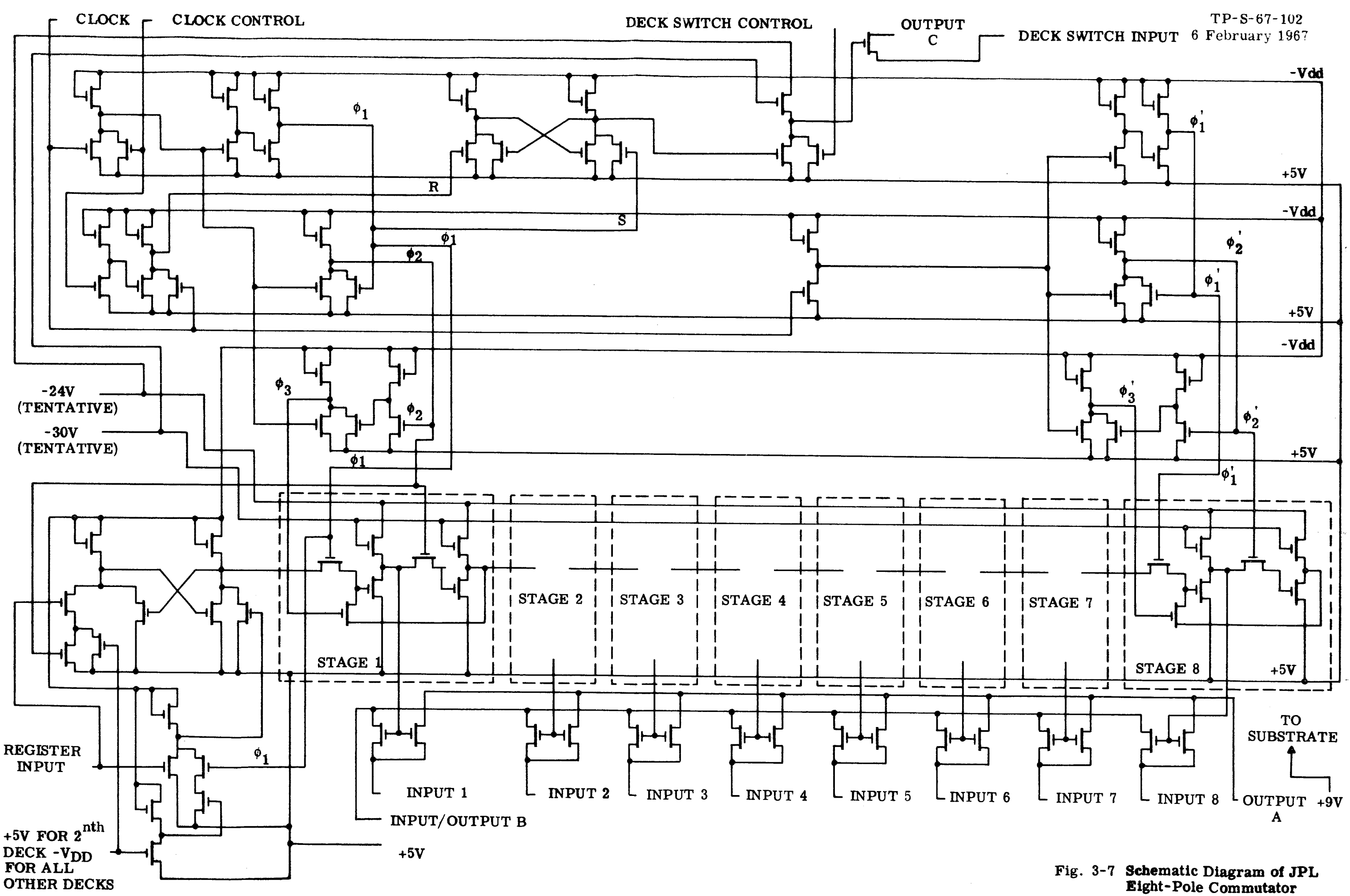


Fig. 3-7 **Schematic Diagram of JPL Eight-Pole Commutator**

Section 4
TECHNICAL PROBLEMS

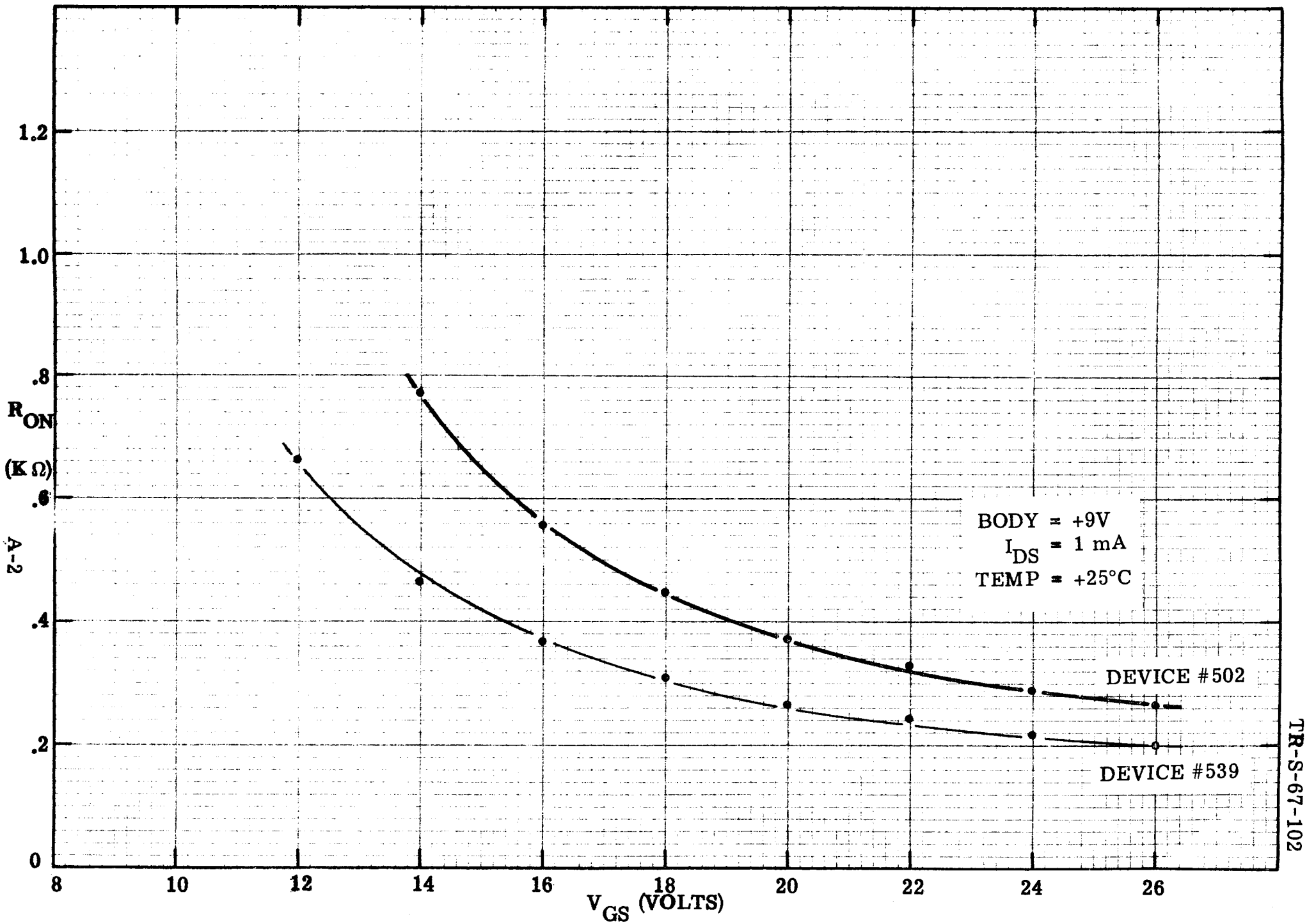
No technical problems of any importance arose during the reporting period.

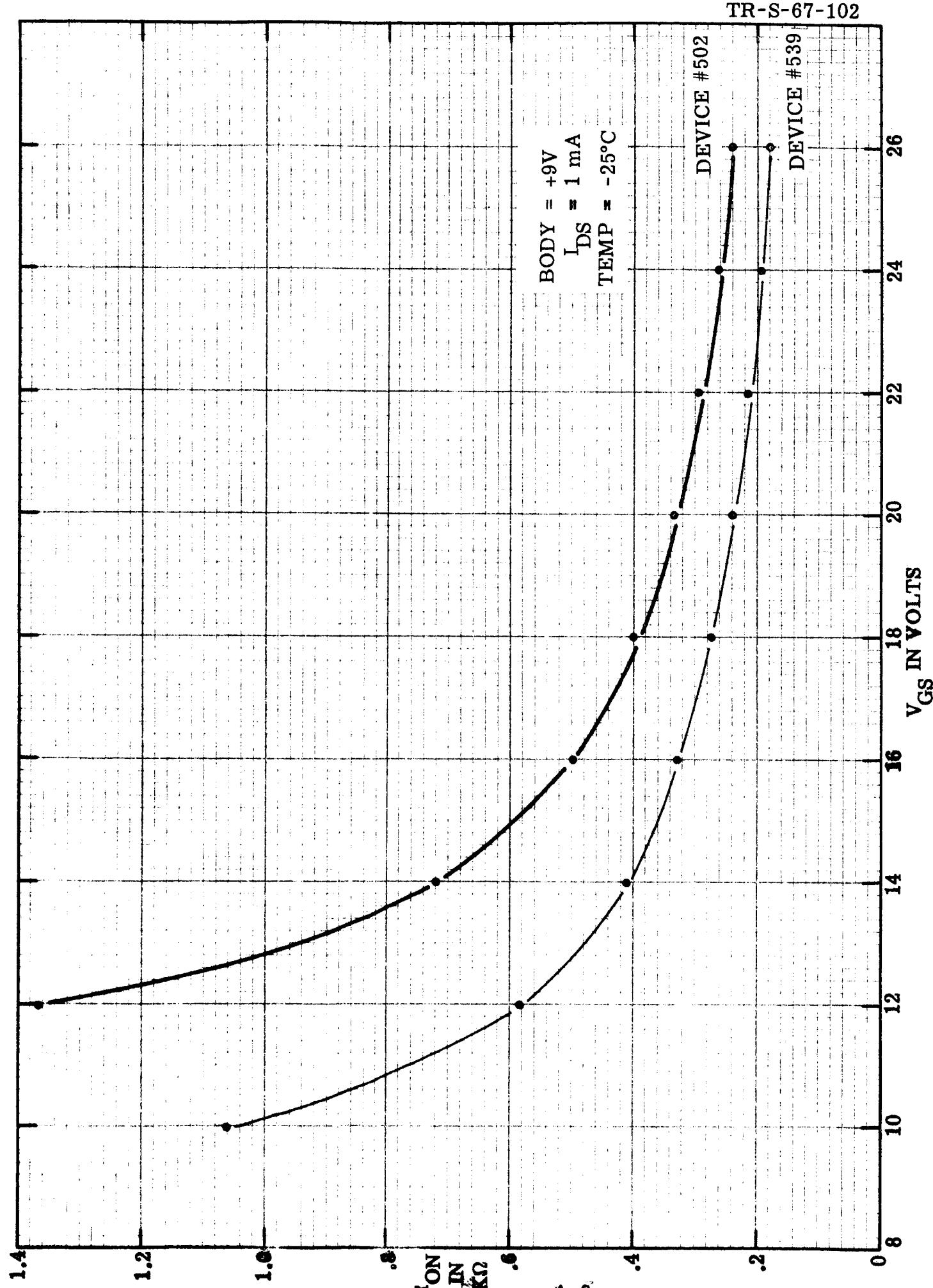
Section 5
WORK PLAN FOR THE NEXT QUARTER

During the next quarter, steps 6 through 8 of the program defined in Section 2 will be started, and steps 1 through 5 should be completed.

Appendix

DATA GRAPHS


1.2
1.0
.8
.6
.4
.2
0
R_{ON}
(K Ω)
8
10
12
14
16
18
20
22
24
26
V_{GS} (VOLTS)
BODY = +9V
I_{DS} = 1 mA
TEMP = +25°C
DEVICE #502
DEVICE #539
A-2
TR-S-67-102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I_{DS} = 1 mA
TEMP = -25°C
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DEVICE #539
R_{ON} IN KΩ
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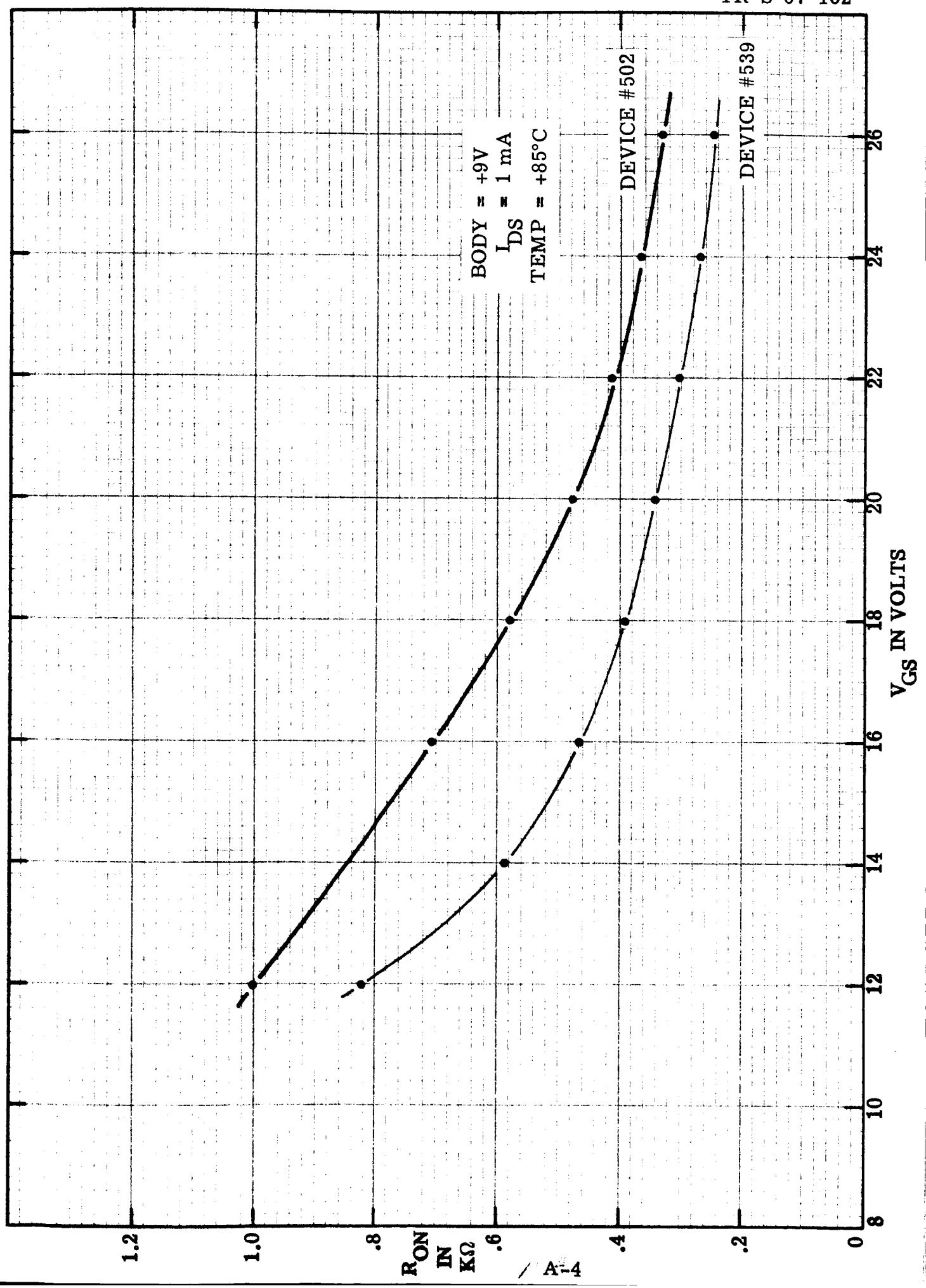
26
V_{GS} IN VOLTS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DEVICE #502
DEVICE #539
R_{ON} IN KΩ
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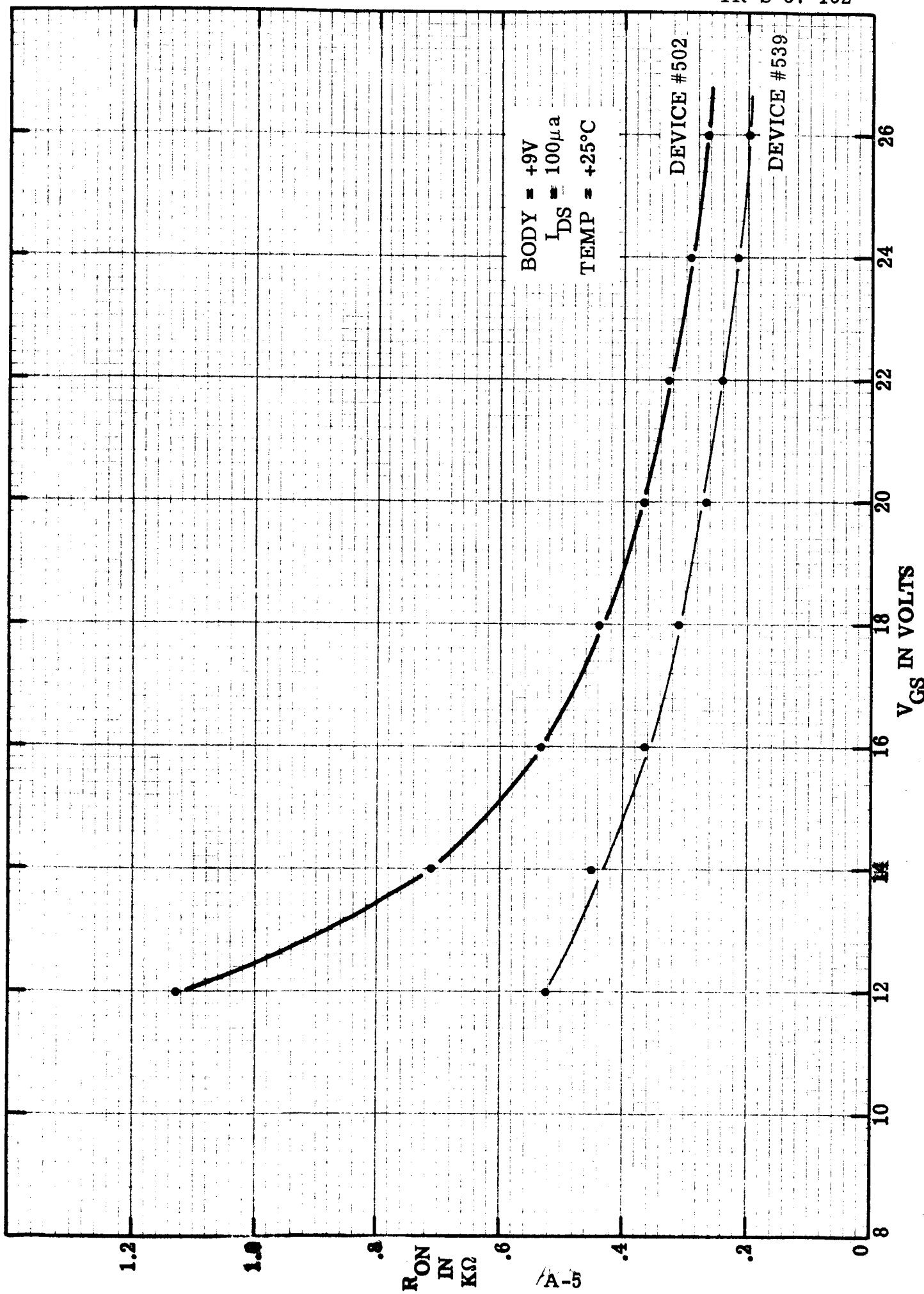
V_{GS} IN VOLTS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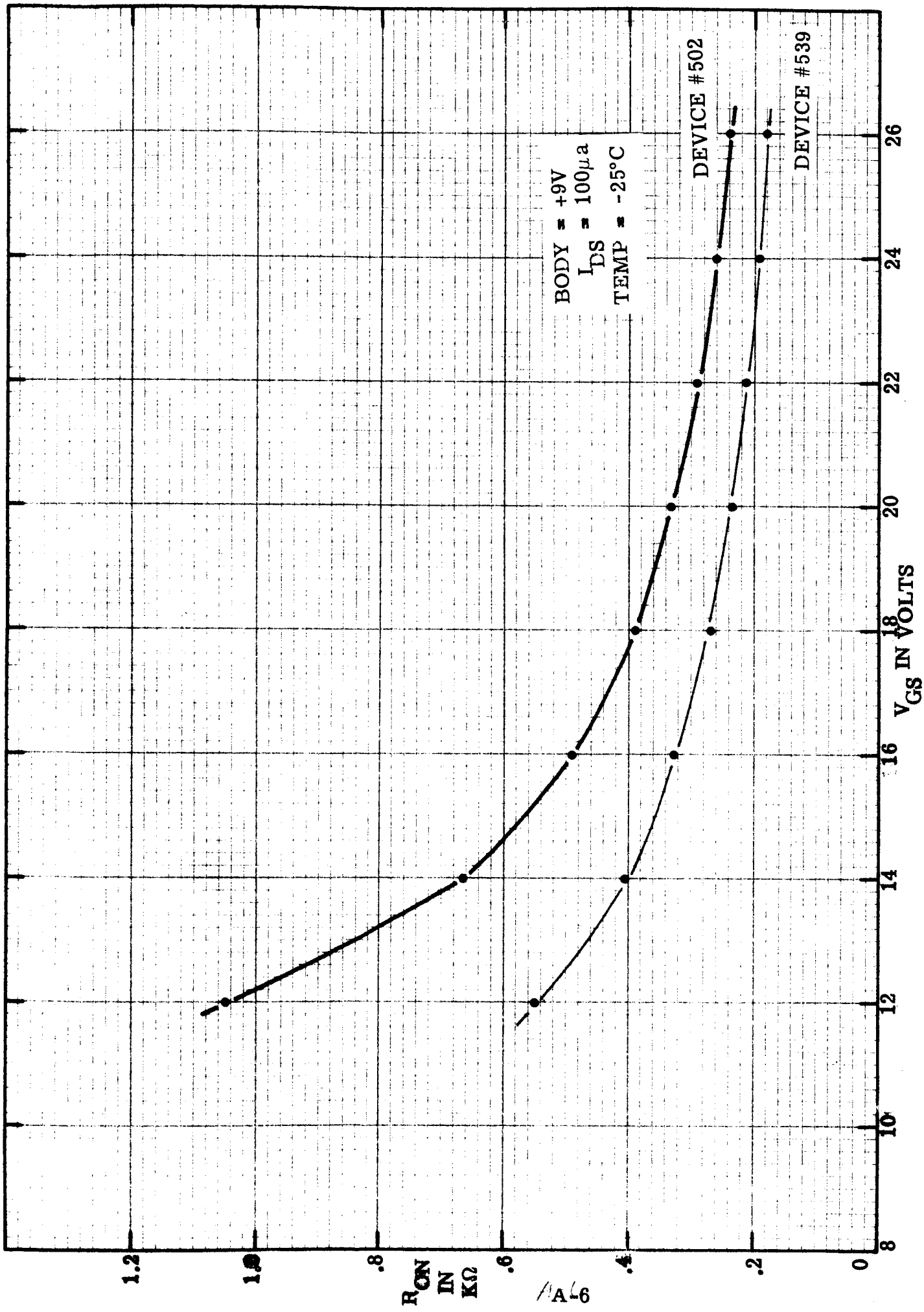
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V_{GS} IN VOLTS
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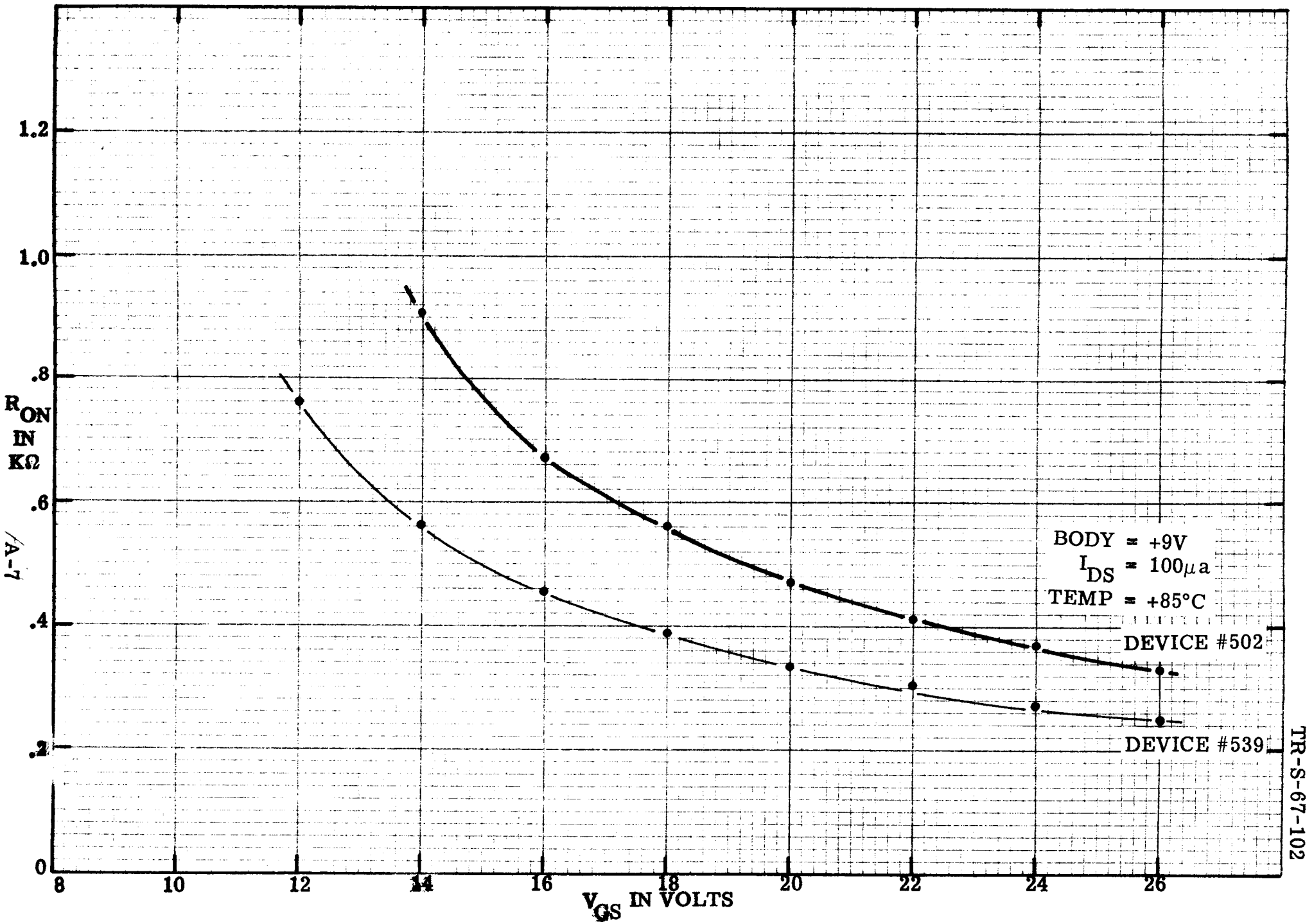
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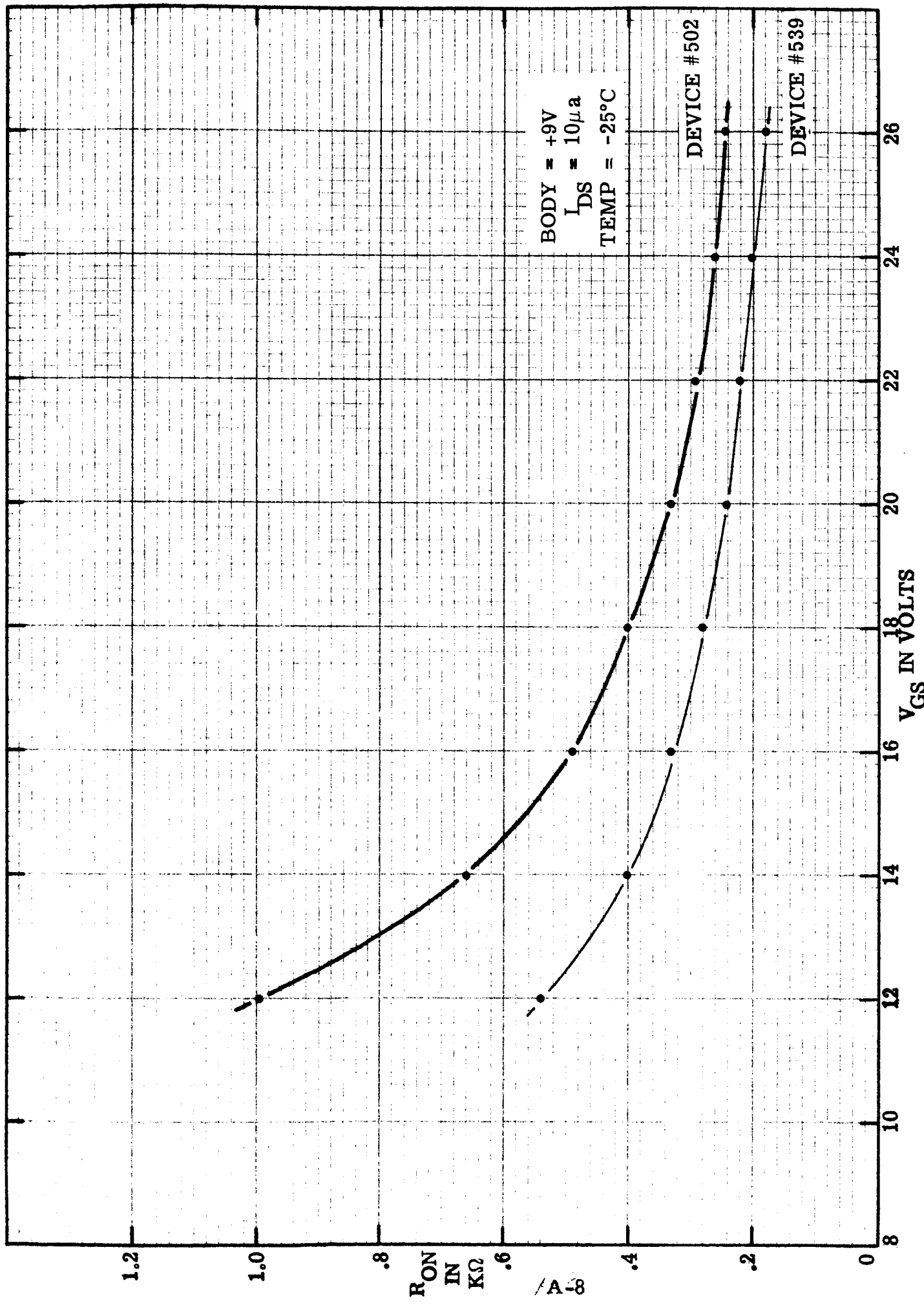
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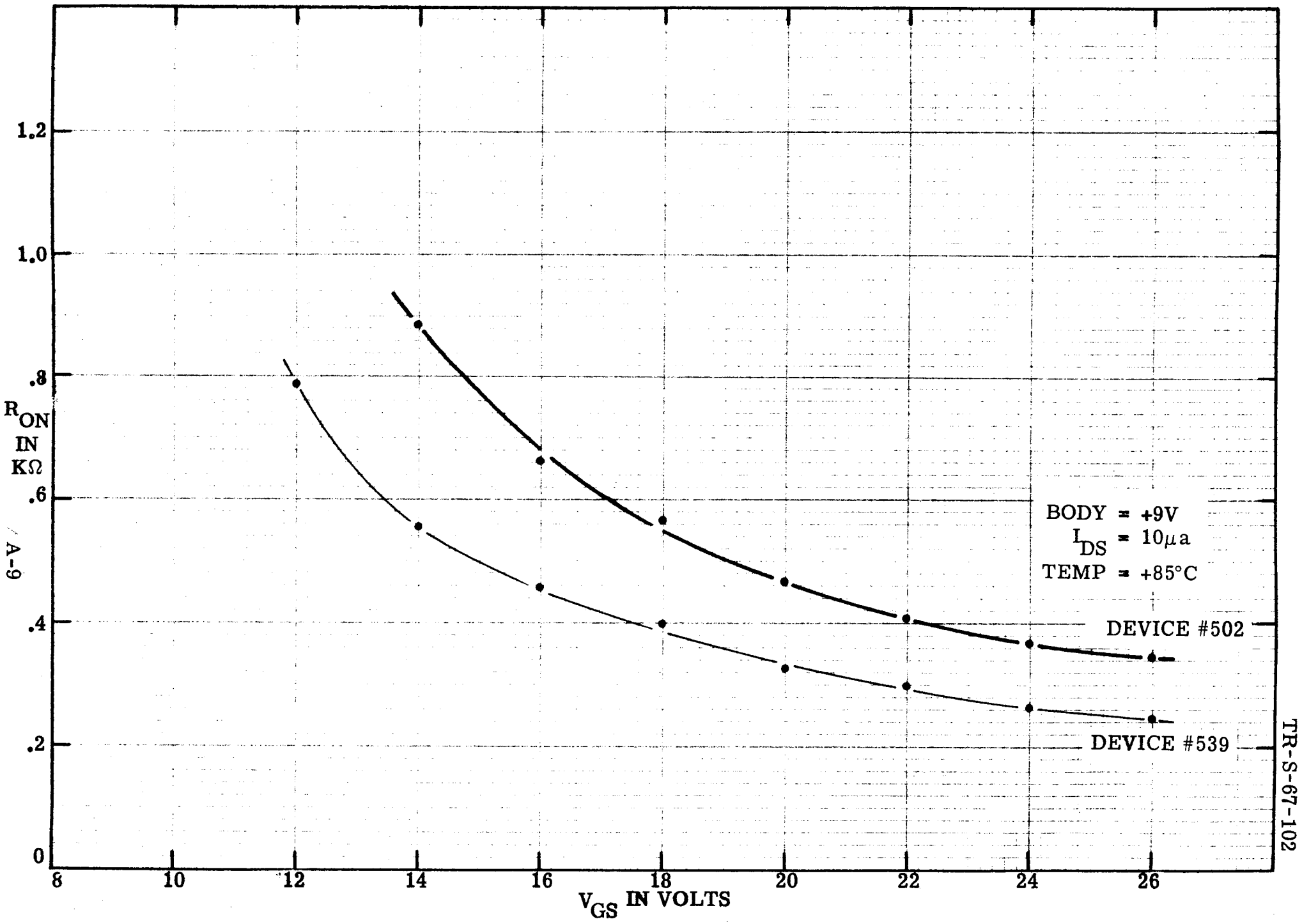
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R_{ON} IN KΩ
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V_{GS} IN VOLTS
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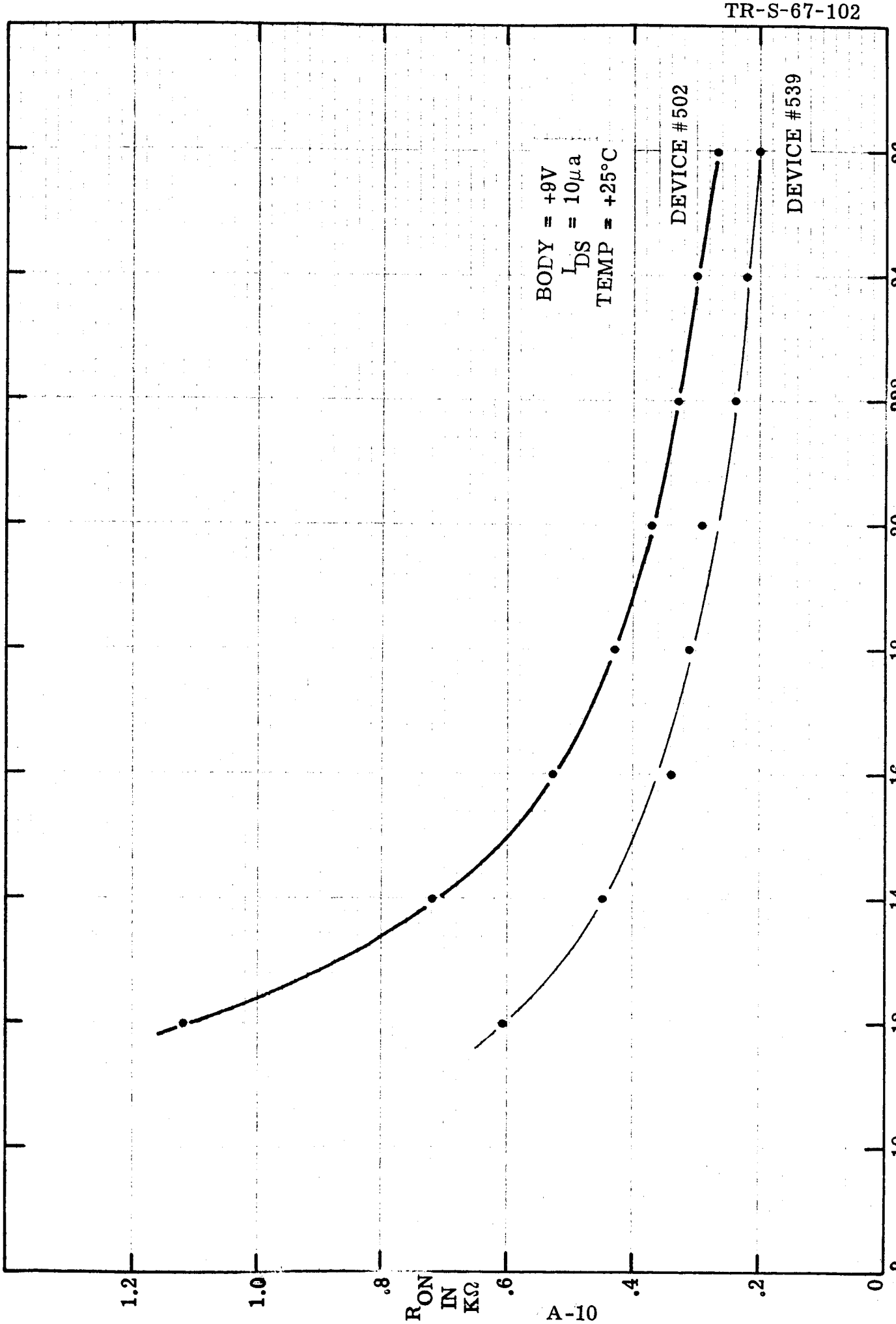
DEVICE #502
DEVICE #539
TR-S-67-102
A-9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DEVICE #539
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